TRENTON Technology Inc.
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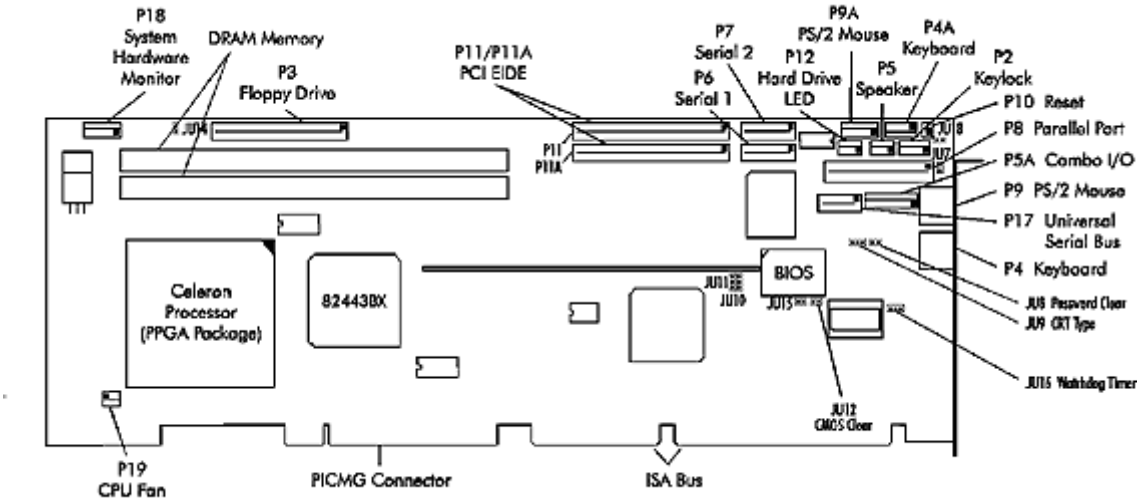
Technical Information – Jumpers, Connectors and Memory
CBX BASIC (5690-x2x) System Host Board

Layout Diagram



Jumpers & LEDs

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "RIGHT" is toward the bracket end of the board; "LEFT" is toward the memory sockets.

JU7 COMBO I/O (P5A) SPEAKER CONNECT

(Also refer to JU18 - Combo I/O Reset Connect.)

INSTALL= Connect speaker data signal to pin 8 of Combo I/O connector (P5A) *

REMOVE= Disconnect

JU8 Password Clear

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

JU9 CRT TYPE SELECT

LEFT = Monochrome
RIGHT = Color *

JU10/11 SYSTEM FLASH ROM OPERATIONAL MODES

The Flash ROM has two programmable sections: the Boot Block for "flashing" in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

	JU10	JU11
Write Protect	Top	Top
Normal PnP (Program Main Block)	Bottom *	Top *
Program All (Boot and Main)	Bottom	Bottom

JU12 CMOS Clear

INSTALL = Clear CMOS
REMOVE = Operate *

NOTE: The CMOS Clear jumper works on power-up. To clear the CMOS, power down the system, install the jumper, then turn the power back on. CMOS is cleared during the POST routines. Then power down the system again and remove the jumper before the next power-up.

JU14 FAN SPEED MONITOR

This jumper *must* be removed (disabled).

JU15 3.3V MONITOR ENABLE

INSTALL = Enable 3.3V monitor
REMOVE = Disable monitor *

NOTE: JU15 enables the 3.3V monitor, which monitors the 3.3V power plane of the backplane. This voltage is routed to the SBC via the PICMG® connector. The monitor generates a RESET to the SBC if 3.3V is below tolerance. If your system does *not* supply 3.3V to the backplane, this jumper *must* be removed (disabled).

JU16 WATCHDOG TIMER

LEFT = Normal reset *
RIGHT = Enable watchdog

JU18 COMBO I/O (P5A) RESET CONNECT

(Also refer to JU7 = Combo I/O Speaker Connect.)

INSTALL= Connect reset data signal to pin 1 of Combo I/O connector (P5A) *

REMOVE= Disconnect

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Connectors

NOTE:
Pin 1 on the connectors is indicated by the square pad on the PCB.

P2 - KEYLOCK CONNECTOR

5 pin single row header, Amp #640456-5

PIN	SIGNAL
1	LED Power
2	Key
3	Gnd
4	Keylock Data
5	Gnd

P3 - FLOPPY DRIVE CONNECTOR

34 pin dual row header,
Robinson Nugent #IDH-34LP-S3-TR

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

P9 - PS/2 MOUSE CONNECTOR

6 pin mini DIN, Kycon #KMDG-6S-BS-PS

PIN	SIGNAL
1	Ms Data
2	Reserved
3	Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

P9A - PS/2 MOUSE HEADER

6 pin single row header, Amp #640456-6

PIN	SIGNAL
1	Ms Data
2	Reserved
3	Kbd Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

P10 - EXTERNAL RESET CONNECTOR

2 pin header, Amp #640456-2

PIN	SIGNAL
1	External Reset In (Low Active)
2	Gnd

P11 - PRIMARY IDE HARD DRIVE CONNECTOR

40 pin dual row header,
Robinson Nugent #IDH-40LP-S3-TR

PIN	SIGNAL	PIN	SIGNAL
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12

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Connectors (Continued)

P4 - KEYBOARD CONNECTOR

6 pin mini DIN, Kycon #KMDG-6S-BS-PS

PIN	SIGNAL
1	Kbd Data
2	Reserved
3	Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Kbd Clock
6	Reserved

P4A - KEYBOARD HEADER

5 pin single row header, Amp #640456-5

PIN	SIGNAL
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

P5 - SPEAKER PORT CONNECTOR

4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	Speaker Data
2	Key
3	Gnd
4	+5V

P5A - COMBO I/O CONNECTOR

8 pin single row header, Amp #640456-8

PIN	SIGNAL
1	Reset (See JU18 in *Configuration Jumpers* above.)
2	Gnd
3	NC
4	Kbd Clock
5	Kbd Data

13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 0	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDP
29	DACK 0	30	Gnd
31	IRQ 14	32	NC
33	Add 1	34	Gnd
35	Add 0	36	Add 2
37	CS 1P	38	CS 3P
39	IDEACTP	40	Gnd

P11A - SECONDARY IDE HARD DRIVE CONNECTOR

40 pin dual row header,
Robinson Nugent #IDH-40LP-S3-TR

PIN	SIGNAL	PIN	SIGNAL
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 1	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDS
29	DACK 1	30	Gnd
31	IRQ15	32	NC

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6	Kbd Lock Data
7	Kbd Power (+5V fused) with self-resetting fuse
8	Speaker Data

Connectors (Continued)

P6 - SERIAL PORT 1 CONNECTOR

10 pin dual row header, 3M #30310-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-0	6	Clear to Send-I
7	Data Terminal Ready-0	8	Ring Indicator-I
9	Signal Gnd	10	NC

P7 - SERIAL PORT 2 CONNECTOR

10 pin dual row header, 3M #30310-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-0	6	Clear to Send-I
7	Data Terminal Ready-0	8	Ring Indicator-I
9	Signal Gnd	10	NC

P8 - PARALLEL PORT CONNECTOR

26 pin dual row header, 3M #30326-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
33	Add 1	34	Gnd
35	Add 0	36	Add 2
37	CS 1S	38	CS 3S
39	IDEACTS	40	Gnd

P12 - HARD DRIVE LED CONNECTOR

4 pin single row header, Amp #640456-4
(This connector is used for both IDE and SCSI drives. See JU19 in the *Jumpers* section.)

PIN	SIGNAL
1	+5V Pullup
2	Light
3	Light
4	+5V Pullup

P17 - UNIVERSAL SERIAL BUS (USB) CONNECTOR

8 pin dual row header, Molex #702-46-0821
(+5V fused with self-resetting fuses)

PIN	SIGNAL	PIN	SIGNAL
1	+5V - USB0	2	+5V - USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd - USB0	8	Gnd - USB1

P18 - SYSTEM HARDWARE MONITOR CONNECTOR

6 pin single row header, Amp #640456-6

PIN	SIGNAL
1	Gnd
2	GPO (General Purpose Output)
3	CI (Chassis Intrusion Input)
4	FAN1 (Fan 1 Tachometer Input)
5	FAN2 (Fan 2 Tachometer Input)
6	OS# (Temperature Sense Output)

P19 - CPU Fan

3 pin single row header, Molex #22-23-2031

PIN	SIGNAL
1	Gnd

17	Data Bit 7	18	Gnd	2	+12V
19	ACK	20	Gnd	3	Fan Tach
21	Busy	22	Gnd		
23	Paper End	24	Gnd		
25	Slct	26	NC		

Memory

The DRAM interface consists of two dual in-line memory module (DIMM) sockets and supports auto detection of memory up to 512MB of Synchronous DRAM (SDRAM). Minimum memory size is 8MB. The System BIOS automatically detects memory type, size and speed.

The SBC uses industry standard 64-bit or 72-bit wide gold finger DIMM DRAM in two 168-pin DIMM sockets.

NOTE: Memory can be installed in one or both DIMM sockets. If only one DIMM module is used, it must be populated in the top DIMM socket (Bank 1 - BK1). If two modules are used, they must be the same DIMM type, but may be different sizes (see table below). EDO DIMMs are not supported. All DIMMs must have gold contacts.

The SBC supports DIMM memory modules which are PC-100 compliant and have the following features:

- 168-pin DIMMs with gold-plated contacts
- 100MHz SDRAM
- Non-ECC (64-bit) or ECC (72-bit) memory
- 3.3 volt only
- Single or double-sided DIMMs in the sizes listed below
- Buffered or Registered configuration

DIMM Size	DIMM Type	Non-ECC	ECC
8 MB	Unbuffered	1M x 64	1M x 72
16 MB	Unbuffered	2M x 64	2M x 72
32 MB	Unbuffered	4M x 64	4M x 72
64 MB	Unbuffered	8M x 64	8M x 72
128 MB	Unbuffered	16M x 64	16M x 72
256 MB	Registered	32M x 64	32M x 72

All memory components and DIMMs used with the SBC must be PC-100 compliant, which means that they comply with Intel's PC SDRAM specifications. These include the PC SDRAM Specification (memory component specific), the PC Unbuffered DIMM Specification, the PC Registered DIMM Specification and the PC Serial Presence Detect Specification. The PC SDRAM specifications can be found at Intel's Developer's web site at http://developer.intel.com/design/pcisets/memory.